2. (Original) A data transmission system as defined in Claim 1, wherein the bidirectional terminal of each of the plurality of processors is coupled to the common node and the common node is coupled through a resistance to a voltage, V^+, so that in the absence of an alarm signal at all the processor inputs, the voltages at the bidirectional terminals of the processors approaches V^+.

3. (Original) A data transmission system as defined in Claim 2, wherein as a result of an error signal at the input of any processor, the voltages at the bidirectional terminals of all the processors approach a reference voltage.

4. (Currently Amended **[Proposed]**) In an information transmission system for transmitting an information payload that comprises a plurality of concatenated signals that are demultiplexed into a plurality of concatenated processors, processed in a plurality of processors, and then multiplexed in a multiplexer, a method of inserting an alarm signal comprising the steps:

(a) detecting an error at one of the processors;

(b) **causing at least one of said concatenated processors to assert** ~~**asserting**~~ a logic level at a bidirectional terminal of the processor at which the error is detected;

(c) coupling the asserted logic level to a respective bidirectional terminal of each of the other processors; and

(d) causing an alarm signal to appear at the outputs of all the processors **in response to said asserted logic level**.

5. (Original) A method as defined in Claim 4, wherein the alarm signals are applied to the multiplexer.

6. (Original) A method as defined in Claim 4, wherein the method is performed only when a concatenation signal is received that signifies that signals distributed to the processors constitute a concatenated payload.

7. (Currently Amended **[Proposed]**) A pointer processor for an information transmission system, the pointer processor comprising:

an input terminal for coupling to an output of a demultiplexer;

an output terminal for coupling to an input of a multiplexer;

a bidirectional terminal coupled to a common node; and

alarm means coupled to the input terminal, to the output terminal and to the bidirectional terminal for:

(i) causing a predetermined logic level to be asserted at the common node in response to an error signal at the processor input, and

(ii) causing an alarm signal to appear at the processor output in response to the application of the predetermined logic level at the processor bidirectional terminal **by said pointer processor**.

8. (Original) A pointer processor as defined in Claim 7, wherein the alarm means includes an error detector for detecting an error in a signal that is included as a component of a concatenated payload.

9. (Original) A pointer processor as defined in Claim 8, wherein the error detector detects the presence of an STS-Nc signal.

10. (Original) A pointer processor as defined in Claim 8, wherein the error detector detects one or more of the following errors in a SONET-compliant system: LOS, LOF, AIS_L and LOP.

11. (Original) A pointer processor as defined in Claim 7, wherein the alarm means comprises:

an error detector;

a wired-OR logic element coupled between the error detector and the bidirectional terminal; and

a combinational logic element having inputs respectively coupled to the error detector and the wired-OR logic element and an output coupled to the output of the processor.

12. (Original) A pointer processor as defined in Claim 11, wherein the error detector detects the presence of an STS-Nc signal.

13. (Previously Presented) A data transmission system for transmitting a payload constituted from a number of concatenated signals, the system comprising:

a demultiplexer having an input for coupling to the payload and having plurality of outputs;

a multiplexer have a plurality of inputs;

a plurality of pointer processors, each having an input coupled to a respective output of the demultiplexer and having an output coupled to a respective input of the multiplexer, wherein

each of the pointer processors comprises:

(a) a bidirectional terminal coupled to a common node, and

(b) circuitry coupled to the processor input, processor output and bidirectional terminal, the circuitry for:

(i) causing a logic level to be asserted at the common node in response to an error signal at the processor input, and

(ii) causing an alarm signal to appear at the processor output in response to the application of a logic level signal at the processor bidirectional terminal, and

the bidirectional terminal of each of the plurality of processors is coupled to the common node and the common node is coupled through a resistance to a voltage, V^+, so that in the absence of an alarm signal at all the processor inputs, the voltages at the bidirectional terminals of the processors approaches V^+.

14. (Previously Presented) A data transmission system as defined in Claim 13, wherein as a result of an error signal at the input of any processor, the voltages at the bidirectional terminals of all the processors approach a reference voltage.

15. (Previously Presented) A pointer processor for an information transmission system, the pointer processor comprising:

an input terminal for coupling to an output of a demultiplexer;

an output terminal for coupling to an input of a multiplexer;

a bidirectional terminal coupled to a common node; and

alarm means coupled to the input terminal, to the output terminal and to the bidirectional terminal for:

(i) causing a predetermined logic level to be asserted at the common node in response to an error signal at the processor input, and

(ii) causing an alarm signal to appear at the processor output in response to the application of the predetermined logic level at the processor bidirectional terminal, and

wherein the alarm means comprises

an error detector,

a wired-OR logic element coupled between the error detector and the bidirectional terminal, and

a combinational logic element having inputs respectively coupled to the error detector and the wired-OR logic element and an output coupled to the output of the processor.

16. (Previously Presented) A pointer processor as defined in Claim 15, wherein the error detector detects the presence of an STS-Nc signal.